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24998	7590	12/07/2004	EXAMINER	
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP			DEB, ANJAN K	
2101 L Street, NW			ART UNIT	
Washington, DC 20037			PAPER NUMBER	
			2858	

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/808,140

Applicant(s)

CORR, WILLIAM E.

Examiner

Anjan K Deb

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AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 September 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-33,35-47 and 49-52 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-5,12-19,22-28,31-33,35-42,45,50 and 51 is/are rejected.
- 7) ☒ Claim(s) 6-11,20,21,29,30,43,44,46,47,49 and 52 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. In response to applicant's arguments regarding rejection of Claim 1 under 35 U.S.C. 102(b) as being anticipated by Yasui et al. (US 4,278,971), that Yasui et al. does not teach "disconnecting said test circuit from respective voltage terminals providing said first and second voltage levels; and measuring said parameter of said circuit under test with said test circuit," applicant is kindly referred to Yasui et al. (column 4 lines 34-37)(Fig. 1) wherein Yasui et al. teach disconnecting conductors (1b,1c) which are used for supplying power to the first and second portion of test circuit for charging capacitors (condensers) 6 and 10 in the first and second portion respectively, furthermore Yasui et al. also teach the step of "measuring said parameter of said circuit under test with said test circuit" (column 4 lines 50-55) wherein Yasui et al. clearly state that an indicator lamp 18 is lit prior to start of the vehicle (before starting vehicle switch 1a is open) for detecting a defective capacitor 6. In view of the above Yasui et al. teach all of the limitations in claim 1, and therefore rejection of Claim 1 under 35 U.S.C. 102(b) is proper as being clearly anticipated by Yasui et al.
2. In response to applicant's arguments regarding rejection of Claim 51 under 35 U.S.C. 102(b) as being anticipated by Yasui et al. (US 4,278,971), that Yasui et al. does not teach the claimed comparator, applicant is kindly referred to Fig. 1 wherein Yasui et al. clearly show a comparator 12 coupled to a power source 1. As shown in Fig. 1, the power source 1 is coupled (connected) to first input (+) of comparator 12 by conductor 1b, diode 9 and resistor 8. The first input (+) of comparator 12 is used for receiving a sensed voltage (voltage at node

A), and a second input (-) of comparator 12 is used for receiving a reference voltage (voltage at node B). Yasui et al. clearly show in Fig. 1, a first storage capacitor (condensor) 6 coupled to power source 1, said first storage capacitor (condensor) 6 being used for storing a voltage supplied by said power source 1, and also for supplying power to said comparator 12 when said comparator is disconnected from said power source. As disclosed by Yasui et al. the power source may be disconnected by opening switch 1a, or by disconnection of conductors (1b, 1c) that are used for connection of power source to comparator 12. As regard to semiconductor die recited in the preamble, the body of the claim following the preamble is a self-contained description of an electric circuit structure and does not depend on the preamble for completeness, therefore the recitation of semiconductor die in the preamble does not limit the claim. In view of the above Yasui et al. teach all of the limitations in claim 51, and therefore rejection of Claim 51 under 35 U.S.C. 102(b) is proper as being clearly anticipated by Yasui et al.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3-5, 12-14, 17-19, 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Yasui et al. (US 4,278,971).

Re claims 1,51 Yasui et al. discloses method for measuring a parameter of a circuit under test (Fig. 1), comprising charging a first portion 6 of test circuit up to a first voltage level (voltage at node A), charging a second portion 10 of said test circuit up to a second voltage level (voltage at node B), disconnecting (switch 1a open)(conductors 1b,1c are disconnected) test circuit from respective voltage terminals providing first and second voltage levels, and measuring (18), (indicating lamp) parameter (High or Low level) of circuit under test with test circuit.

Re claims 3-5, Yasui et al. discloses charging a first portion comprises charging a first capacitor 6 of said test circuit to a power rail voltage level (voltage at node A is considered rail voltage), and wherein said act of charging a second portion comprises charging a second capacitor 10 of said test circuit to a predetermined reference voltage level.

Re claims 12-14, Yasui et al. discloses disconnecting test circuit from power rail (switch 1a open).

Re claims 17, 19, Yasui et al. discloses act of measuring comprises comparing a sensed voltage with a reference voltage. Voltage at node B is considered reference voltage.

Re claim 18, Yasui et al. discloses act of comparing comprises comparing voltage sensed at a ground terminal (node C) of said circuit under test with a reference voltage.

Re claim 51, Yasui et al. disclose at least one circuit 6 to be tested, at least one test circuit (12,16,17,18) for measuring a parameter of said at least one circuit 6 to be tested, said at least one test circuit comprising: a comparator 12 coupled to a power source 1, said comparator 12 having a first input (+) for receiving a sensed voltage (voltage at node A) and a second input (-) for receiving a reference voltage (voltage at node B), a first storage capacitor 6 coupled to said power source 1 and also coupled to said comparator 12, said first storage capacitor (condensor) 6 being used for storing a voltage supplied by said power source and also for providing power to said comparator when said comparator is disconnected from said power source. As shown in Fig. 1, the power source 1 is coupled (connected) to first input (+) of comparator 12 by conductor 1b, diode 9 and resistor 8. The first input (+) of comparator 12 is used for receiving a sensed voltage (voltage at node A), and a second input (-) of comparator 12 is used for receiving a reference voltage (voltage at node B). Yasui et al. further disclose a second storage capacitor 10 coupled to a reference voltage source (power source 1 is considered a reference voltage source) and also coupled (by conductor 1b and resistor 11) to said second input (-) of said comparator 12 said second storage capacitor (condensor) 10 being used for storing a reference voltage provided by said reference voltage source and also for providing said second input of said comparator with said reference voltage (column 2 lines 59-60) when said comparator is disconnected from said reference voltage source. As disclosed by Yasui et al. the power source may be disconnected by opening switch 1a, or by disconnection of conductors (1b, 1c) that are used for connection of power source to comparator 12. As regard to semiconductor die recited in the preamble, the body of the claim following the preamble is a self-contained description of an electric circuit structure

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and does not depend on the preamble for completeness, therefore the recitation of semiconductor die in the preamble does not limit the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 22, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui et al. (US 4,278,971) in view De Jong (US 6,664,798).

Re claims 22, 23 Yasui et al. discloses all of the claimed limitations as set forth above except quantifying ground bounce and quantifying power droop of circuit under test.

De Jong et al. disclose test circuit for testing integrated circuit comprising quantifying ground bounce and power droop for said circuit under test.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Yasui et al. by adding comparator with variable threshold disclosed by De Jong et al. for quantifying ground bounce and power droop for said circuit under test.

7. Claims 15, 16, 24-28, 31, 32, 35-41, 45, 49, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui et al. (US 4,278,971) in view of Frech et al. (US 2002/0125897).

Re claims 15, 16, 24-28, 31, 32, 35, 36, 40 Yasui et al. discloses all of the claimed limitations as set forth above except respective switches within first and second charging

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portions for disconnecting test circuit from terminals respectively providing said first and second voltage levels.

Frech et al. discloses method of quantifying on-chip power supply integrity comprising disconnecting 102 test circuit C_s from terminals respectively providing said first and second voltage levels. Switch 102 is broadly interpreted as transistor switch.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Yasui et al. by adding a transistor switch (switching capacitor) disclosed by Frech et al. for disconnecting test circuit from terminals respectively for testing on-chip power supply integrity.

Re claim 36, Yasui et al. disclose comparator 12 comprises an output for producing a signal when said parameter, as measured, has a predetermined relationship with a reference voltage.

Re claim 37, Yasui et al. did not expressly disclose test circuit is integrated onto a semiconductor die.

Frech et al. discloses method of quantifying on-chip power supply integrity comprising integrated circuits. Integrated circuit is broadly interpreted as semiconductor die.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Yasui et al. by adding test circuit integrated onto a semiconductor die disclosed by Frech et al. for testing on-chip power supply integrity.

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Re claims 38, 39, Yasui et al. discloses all of the claimed limitations including charging first 10 and second 6 circuit portion to first and second voltage level respectively, except respective switches within first and second circuit portion.

Frech et al. discloses method of quantifying on-chip power supply integrity comprising respective switches 102 within first and second circuit portions (partitions)(page 3 para 0028).

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Yasui et al. by adding respective switches disclosed by Frech et al. for testing on-chip power supply of each partitioned circuit.

Re claim 41 Yasui et al. discloses measuring portion comprises a comparator 12.

Re claim 45 Yasui et al. discloses second input of comparator 12 coupled to terminal A providing second voltage level, said terminal being reference voltage terminal for providing a reference voltage, said comparator comparing said reference voltage and said sensed parameter (voltage at node B) of said at least one circuit to be tested.

Re claim 49, Yasui et al. discloses second charging portion comprises a second storage capacitor 10 for providing said reference voltage to said second input (node B) when said second input is disconnected (switch 1a open) from said reference voltage terminal.

Allowable Subject Matter

8. Claims 6-11, 20, 21, 29, 30, 43, 44, 46, 47, 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Indicating Allowable Subject Matter

9. The following is an examiner's statement of reasons for indicating allowable subject matter:

Claims 6-11 are allowable because the prior art does not teach changing predetermined reference voltage and repeating steps (a) through (d) if measured parameter does not have a predetermined relationship with said predetermined reference voltage.

Claims 20,21 is allowable because the prior art does not teach act of comparing comprises toggling a state of a transistor.

Claims 29,30,43,44 are allowable because the prior art does not teach a switch comprising a transistor coupled between first input of comparator and circuit under test.

Claims 46,47 are allowable because the prior art does not teach a switch coupled between second input of comparator and reference voltage terminal.

Claim 52 is allowable because the prior art does not teach the claimed first, second, and third transistor for toggling comparator in and out of electrical contact with circuit to be tested, reference voltage source and power source respectively.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Watson (US 4,831,325) discloses method of measuring a parameter of a circuit (Fig. 1) in a semiconductor device comprising charging a first portion C_x of test circuit up to a first voltage level (v_i), charging a second portion C_r of said test circuit up to a second voltage level (v_0), disconnecting (switch 1,2 open) test circuit from respective voltage terminals (3,4) providing first (v_i) and second voltage levels (v_0), and measuring (7), parameter of circuit under test with test circuit.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,


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however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Anjan K. Deb whose telephone number is 571-272-2228. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le, can be reached at (571) 272-2233.



Anjan K. Deb

Patent Examiner

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12/2/04

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